In the Claims:

1. (Currently Amended) A power synthesizer comprising~~:~~

~~a first stage having a first modulator and a first discrete amplitude amplifier in series with one another;~~

~~a second stage in parallel with the first having a second modulator and a second discrete amplitude amplifier in series with one another; and~~

a plurality of *n* stages in parallel with one another, wherein *n* is an integer at least equal to two, each of the *n* stages comprising:

a modulator and a discrete amplitude amplifier in series with one another,

each n^{th} discrete amplitude amplifier for applying a gain that is unique as compared to all other of the discrete amplitude amplifiers; and

an actuator for simultaneously switching the ~~first and second~~ *n* modulators.

2. (Currently Amended) The power synthesizer of claim 1 wherein each of the ~~first and second~~ *n* discrete amplifiers ~~are~~ comprises a constant envelope amplifier~~s~~.

3. (Currently Amended) The power synthesizer of claim 1 wherein each of the ~~first and second~~ *n* modulators ~~are~~ comprises a continuous phase modulator~~s~~.

4. (Currently Amended) The power synthesizer of claim 3 wherein each of the ~~first and second~~ *n* modulators ~~are~~ comprises a pulse-amplitude modulator~~s~~.

5. (Currently Amended) The power synthesizer of claim 1 further comprising a power combiner having parallel inputs coupled to outputs of the ~~first and second modulators~~ *n* discrete amplitude amplifiers.

6. (Currently Amended) The power synthesizer of claim ~~5~~1, wherein ~~the first amplifier has an input coupled to an output of the first modulator, and the second amplifier has an input~~ , for each of the *n* stages, the discrete amplitude amplifier has an input that is

directly coupled to an output of the ~~second~~ modulator.

7. (Currently Amended) The power synthesizer of claim 1 further comprising a discrete amplitude generator having parallel outputs coupled to ~~respective~~ inputs of the ~~first and second modulators~~ n stages, said discrete amplitude generator for converting a real input to parallel binary outputs.

8. Cancelled.

9. The power synthesizer of claim ~~8~~1, wherein each ~~amplifier~~ of the n stages has an output coupled to an input of a separate transmit antenna.

10. The power synthesizer of claim 1 ~~having n stages in parallel with one another, wherein n is an integer greater than two,~~ wherein

~~each stage has a modulator and an amplifier in series with one another;~~

each of the modulators is coupled to a common actuator; and

each n^{th} amplifier is for outputting a signal amplitude $a_0 / 2^{n-1}$ ~~that is unique as compared to all other of the amplifiers~~, where a_0 is a maximum signal amplitude output by any of said amplifiers,

the power synthesizer further comprising a discrete amplitude generator for converting a real valued input to a first and second parallel binary outputs that are each coupled to an input of the respective first and second modulators.

11. (Currently Amended) The power synthesizer of claim 1 wherein ~~the first~~ , in one stage, the discrete amplitude amplifier comprises x FETs each having a drain and a gate, and in another stage, the discrete amplitude ~~and the second~~ amplifier comprises $x/2$ FETs each having a drain and a gate, wherein x is an integer greater than two, wherein the x FETs of the ~~first~~ discrete amplitude amplifier ~~have coupled~~ of the one stage have coupled in parallel one of gates and drains, and wherein the $x/2$ FETs of the ~~second~~ discrete amplifier of the another stage have coupled in parallel one of gates and drains.

12. (Original) The power synthesizer of claim 1 disposed within a mobile station, further comprising an inverse fast fourier transform IFFT block, said IFFT block for converting an amplitude modulated input to a bit modulated output.

13. (Currently Amended) In a transmitter comprising, in series, an encoder, a serial to parallel converter, a parallel to serial converter for outputting a digital signal at baseband, and at least one transmit antenna, the improvement comprising:

a power synthesizer block comprising at least two discrete amplifier stages in parallel, each stage disposed between the parallel to serial converter and the at least one transmit antenna, and each discrete amplifier stage comprises a discrete amplitude amplifier for applying a gain that differs from that applied by each other discrete amplitude amplifier.

14. (Original) In the transmitter of claim 13, the improvement further comprising an absence of a digital to analog converter disposed between the parallel to serial converter and the power synthesizer block.

15. (Original) In the transmitter of claim 13, wherein each of the at least two discrete amplifier stages comprises a discrete amplitude amplifier and a modulator in series with one another.

16. (Original) In the transmitter of claim 15, the improvement further comprising an inverse fast fourier transform IFFT block disposed between the serial to parallel converter and the parallel to serial converter, the power synthesizer block further comprising a discrete amplitude generator for converting a real valued input from the IFFT block to parallel binary outputs, each parallel binary output coupled to an input of a modulator.

17. (Original) In the transmitter of claim 15, the power synthesizer block further comprising at least one power combiner coupling an output of each of the at least two discrete amplifier stages with the at least one transmit antenna.

18. (Currently Amended) In the transmitter of claim 15, ~~the improvement further~~

~~comprising~~ wherein each of the modulators ~~comprising~~ comprises a continuous phase modulator.

19. (Currently Amended) In the transmitter of claim 15, ~~the improvement further comprising each of the discrete amplifiers comprising~~ wherein each of the discrete amplifiers comprises a constant envelope amplifier.

20. In the transmitter of claim 15, the improvement further comprising:

the at least one transmit antenna comprises a first and a second transmit antenna, wherein an output of one of the at least two discrete amplifier stages is coupled to an input of the first transmit antenna and an output of another of the at least two discrete amplifier stages is coupled to an input of the second transmit antenna.

21. (Original) In the transmitter of claim 20, the improvement further comprising:

the at least two transmit antennas comprise n transmit antennas and the at least two discrete amplifier stages comprise n discrete amplifier stages, wherein each n^{th} transmit antenna is coupled to an output of an n^{th} discrete amplifier stage.

22. (Original) In the transmitter of claim 15, the improvement further comprising the transmitter being disposed within a mobile station or a base station.

23. (Currently Amended) A method of transmitting a signal on a mutlicarrier communication channel comprising:

providing a separate bit of a bit stream on each of n parallel inputs~~;~~ each bit of the bit stream representing a different significance;

for each of the n parallel inputs, controlling a phase of the input bit and amplifying a power of the input bit at a power that is unique respecting all other n parallel inputs;

combining all ~~amplified and~~ n phase controlled and amplified bits in one of a spatial manner and a circuit manner.

24. (Currently Amended) The method of claim 23, wherein combining all amplified and phase controlled bits ~~in a spatial manner~~ comprises simultaneously transmitting at

least two separately amplified and phase controlled bits by separate transmit antennas.

25. (Original) The method of claim 23, wherein controlling a phase of the input bit comprises spectrally shaping the input bit with a continuous phase modulator.

26. (Original) The method of claim 25 wherein the modulator comprises a pulse amplitude modulator.

27. (Original) The method of claim 25 wherein the modulator approximately performs Gaussian minimum shift keying.

28. (Original) The method of claim 25 further comprising, previous to providing a separate bit of a bit stream, converting an amplitude modulated signal to the bit stream.

29. (Currently Amended) The method of claim 23 wherein combining the amplified phase controlled bits in a circuit manner comprises combining all <u>of the *n*</u> amplified and phase controlled bits with at least one power combiner prior to transmission.

30. (New) The power synthesizer of claim 1 wherein each of the *n* discrete power amplifiers apply a gain that differs from that applied by another nearest-power discrete power amplifier by a fixed amount.

31. (New) The power synthesizer of claim 30 wherein the fixed amount is about 6 dB.

32. (New) In the transmitter of claim 13, the improvement further comprising each discrete amplitude amplifier for applying a gain that differs by a fixed amount from that applied by its nearest-gain neighbor amplitude amplifier.

33. (New) In the transmitter of claim 32, the improvement further comprising the fixed amount being about 6 dB.

34. (New) The method of claim 23, wherein amplifying a power of the input bit at a

power that is unique respecting all other *n* parallel inputs comprises, for each of the *n* parallel inputs, amplifying with a power that differs by a fixed amount from a next nearest power amplification.

35. (New) The method of claim 34, wherein the fixed amount is about 6 dB.

36. (New) A power synthesizer comprising:

a plurality of *n* stages in parallel with one another, wherein *n* is an integer at least equal to two, each of the *n* stages comprising modulating means in series with amplitude amplifying means, wherein each of the *n* amplitude amplifying means is for applying a gain that is unique as compared to all other of the *n* amplitude amplifying means; and

actuating means for simultaneously switching the *n* modulating means.

37. (New) The power amplifier of claim 36, wherein the modulating means comprises a modulator, and the amplitude amplifying means comprise an amplitude amplifier.